

# DATA SHEET

## **TDA8706**

**6-bit analog-to-digital converter  
with multiplexer and clamp**

Preliminary specification  
Supersedes data of February 1992  
File under Integrated Circuits, IC02

1996 Aug 20

# 6-bit analog-to-digital converter with multiplexer and clamp

## TDA8706

### FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package.

### APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIP/CO) for TV
- Videophone
- Frame grabber.

### QUICK REFERENCE DATA

Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CCA</sub>	analog supply voltage (pin 2)	4.5	5.0	5.5	V
V <sub>CCD</sub>	digital supply voltage (pin 10)	4.5	5.0	5.5	V
I <sub>CCA</sub>	analog supply current (pin 20)	–	32	39	mA
I <sub>CCD</sub>	digital supply current (pin 10)	–	28	37	mA
ILE	integral linearity error	–	–	±0.75	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
f <sub>CLK</sub>	maximum clock frequency	20	–	–	MHz
P <sub>tot</sub>	total power dissipation	–	300	418	mW
T <sub>amb</sub>	operating ambient temperature range	0	–	+70	°C

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8706	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA8706T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

### GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit Analog-to-Digital Converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

### FUNCTIONAL DESCRIPTION

The TDA8706 is a 'like-flash' converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH). Luminance clamping level is fitted with 00H code (output 000000). Chrominance clamping level is fitted with 20H code (output 100000).

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### BLOCK DIAGRAM

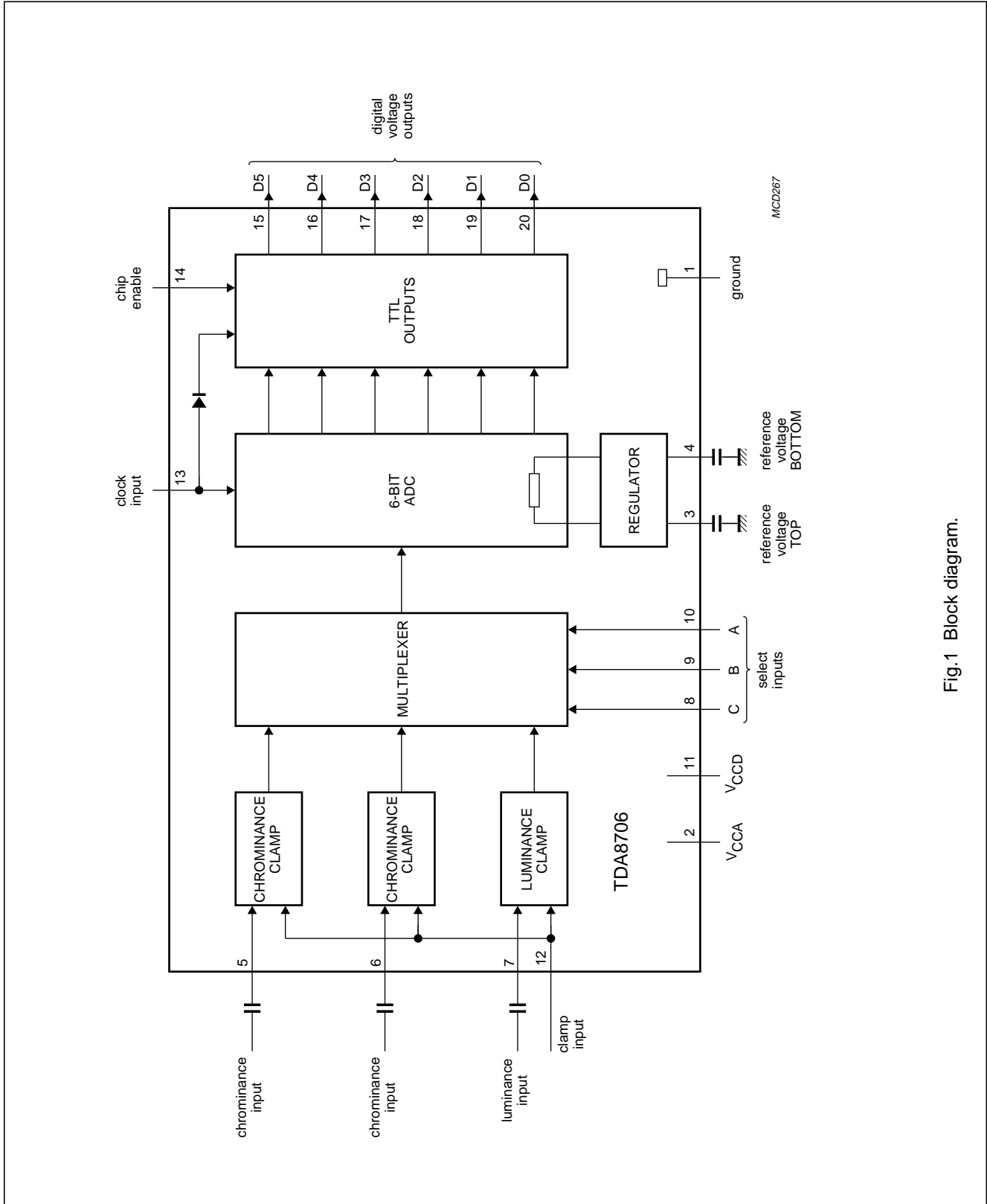


Fig.1 Block diagram.

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### PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V <sub>CCA</sub>	2	analog positive supply (+5 V)
V <sub>RT</sub>	3	reference voltage TOP decoupling
V <sub>RB</sub>	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V <sub>CCD</sub>	11	digital positive supply voltage (+5 V)
CLAMP	12	damp pulse input (positive pulse)
CLK	13	clock input
$\overline{\text{CE}}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage output: significant bit (LSB)

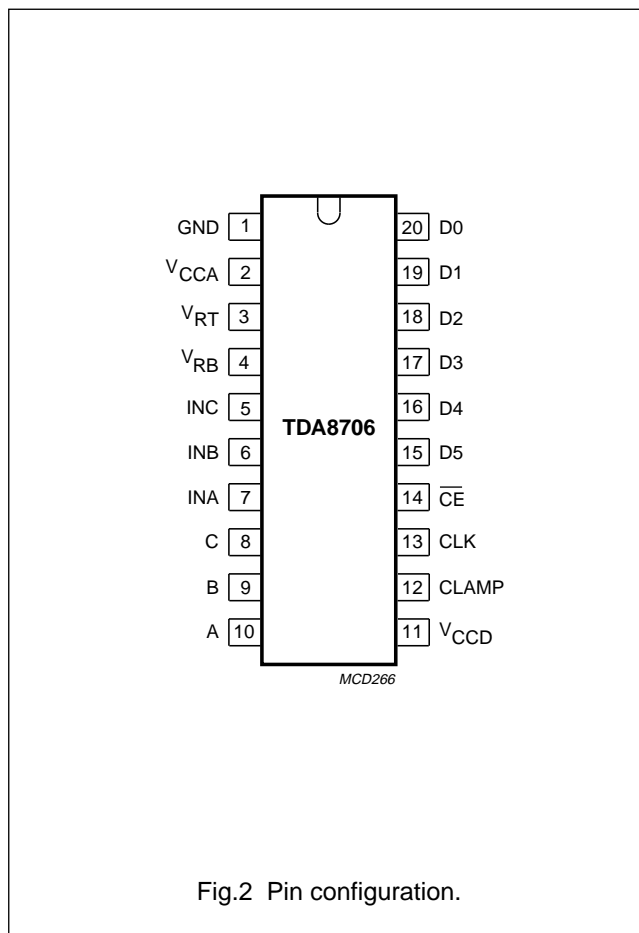


Fig.2 Pin configuration.

**6-bit analog-to-digital converter with  
multiplexer and clamp****TDA8706****LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN.</b>	<b>MAX.</b>	<b>UNIT</b>
$V_{CCA}$	analog supply voltage range (pin 2)	-0.3	+7.0	V
$V_{CCD}$	digital supply voltage range (pin 10)	-0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	1.0	-	V
$V_I$	input voltage range	-0.3	+7.0	V
$I_O$	output current	-	10	mA
$T_{stg}$	storage temperature range	-55	+150	°C
$T_{amb}$	operating ambient temperature range	0	+70	°C

**HANDLING**

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

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**CHARACTERISTICS** (see Tables 1 and 2)

$V_{CCA} = 4.5$  to  $5.5$  V;  $V_{CCD} = 4.5$  to  $5.5$  V =  $V_{CCD}$ ;  $T_{amb} = 0$  to  $+70$  °C;  $C_{VRB} = C_{VR1} = 100$  nF; Typical values measured at  $V_{CCA} = V_{CCD} = 5$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CCA}$	analog supply voltage (pin 2)		4.5	5.0	5.5	V
$V_{CCD}$	digital supply voltage (pin 10)		4.5	5.0	5.5	V
$I_{CCA}$	analog supply current (pin 2)		–	32	39	mA
$I_{CCD}$	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
<b>Inputs</b>						
CLOCK INPUT (PIN 13)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{CLK} = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{CLK} = 2.7$ V	–	–	100	$\mu$ A
$Z_i$	input impedance	$f_{CLK} = 20$ MHz	–	4	–	k $\Omega$
$C_i$	input capacitance	$f_{CLK} = 20$ MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{CLK} = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{CLK} = 2.7$ V	–	–	20	$\mu$ A
<b>Reference voltage (pins 3 and 4)</b>						
$V_{RT}$	reference voltage TOP decoupling		3.22	3.35	3.44	V
$V_{RB}$	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
<b>Analog inputs INA, INB, INC (pins 7, 6 and 5)</b>						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
$Z_i$	input impedance	$f_i = 4.43$ MHz	100	–	–	k $\Omega$
$C_{clamp}$	coupling clamp capacitance		1	10	1000	nF
<b>Analog signal processing (pins 5, 6 and 7) (<math>f_{CLK} = 20</math> MHz)</b>						
$f_1$	fundamental harmonics (full scale)	$f_i = 4.43$ MHz	–	–	0	dB
$f_{all}$	harmonics (full scale); all components	$f_i = 4.43$ MHz	–	–45	–	dB
$G_{diff}$	differential gain	note 1	–	0.4	–	%
$\phi_{diff}$	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Outputs</b>						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (see Table 2)						
$V_{OL}$	LOW level input voltage	$I_O = 1 \text{ mA}$	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_O = 0.5 \text{ mA}$	2.7	–	$V_{CCD}$	V
$I_{OZ}$	output current in 3-state mode	$0.4 \text{ V} < V_O < V_{CCD}$	–20	–	+20	$\mu\text{A}$
<b>Switching characteristics</b>						
CLOCK TIMING (see Fig.3)						
$f_{CLK}$	maximum clock frequency		20	–	–	MHz
$f_{mux}$	maximum multiplexing frequency		10	–	–	MHz
$t_{CLK}$	period		50	–	–	ns
	duty cycle	$CLK = V_{IH}$	45	50	66.6	%
$t_{LOW}$	LOW time	at 50%	16	–	–	ns
$t_{HIGH}$	HIGH time	at 50%	22.5	–	–	ns
$t_{CLR}$	rise time	at 10 to 90%	4	6	–	ns
$t_{CLF}$	fall time	at 90 to 10%	4	6	–	ns
<b>Select signals, Clamp, Data</b> (see Figs 4 and 5)						
$t_S$	set-up time select A, B and C		35	–	–	ns
$t_r$	rise time A, B and band C	at 10 to 90%	4	6	–	ns
$t_f$	fall time A, B and band C	at 90 to 10%	4	6	–	ns
$t_{CLPS}$	set-up time clamp asynchronous		0	–	–	
$t_{CLPH}$	hold time clamp asynchronous		0	–	–	
$t_{CLPP}$	clamp pulse	$C_{CLP} = 10 \text{ nF}$	–	3	–	$\mu\text{s}$
$t_d$	data output delay time		–	15	24	ns
$t_{DH}$	data hold time		12	–	–	ns
<b>Transfer function</b>						
ILE	DC integral linearity error		–	–	$\pm 0.75$	LSB
DLE	DC differential linearity error		–	–	$\pm 0.5$	LSB
AILE	AC integral linearity error	note 3	–	–	$\pm 2$	LSB
EB	effective bits	note 3	–	5.7	–	bits
<b>Timing</b>						
DIGITAL OUTPUTS						
$T_{dt}$	3-state delay time	see Fig.6	–	16	25	ns
$T_{sto}$	sampling time offset		–	2	–	ns

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Notes to the characteristics

1. Low frequency ramp signal ( $V_{VI(p-p)} = 1.8\text{ V}$  and  $f_i = 15\text{ kHz}$ ) combined with a sine wave input voltage ( $V_{VI(p-p)} = 0.5\text{ V}$  and  $f_i = 4.43\text{ MHz}$ ) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

$$SVRR = 20 \log \frac{\Delta V_{Vi(31)}}{\Delta V_{CCA}}$$

3. Full-scale sine wave;  $f_i = 4.43\text{ MHz}$ ,  $f_{CLK} = 20\text{ MHz}$ .

Table 1 Output coding

STEP	VI <sup>(1)</sup>	BINARY OUTPUTS
	(TYP. VALUE)	D5 TO D0
Underflow	<2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		.....
.		.....
.		.....
62	3.072 V	111110
63	3.086 V	111111
Overflow	>3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 TO D5
1	high impedance
0	active; binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	V <sub>inA</sub>
0	1	X <sup>(1)</sup>	2.2
1	1	0	2.2

Note

1. X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	V <sub>inB</sub> /V <sub>inC</sub>
0	1	X <sup>(1)</sup>	2.65
1	1	32	2.65

Note

1. X = don't care.



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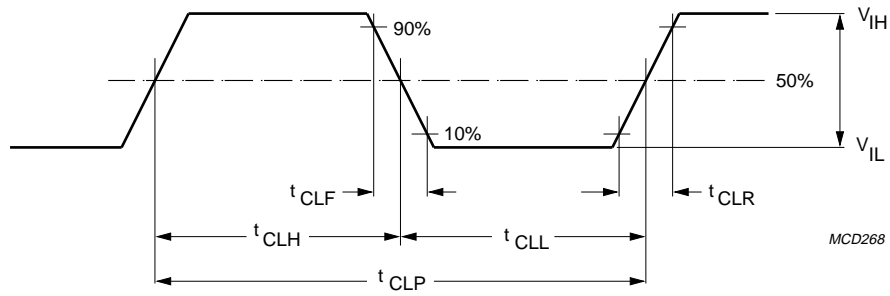


Fig.3 AC clock characteristics.

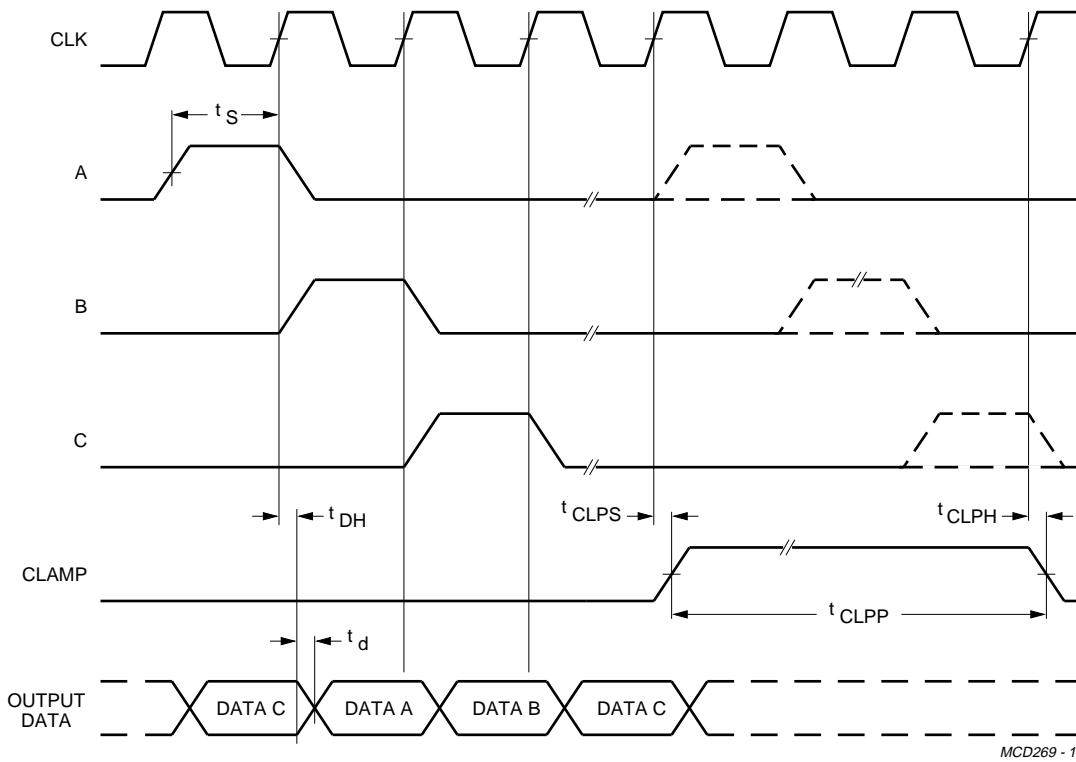


Fig.4 AC characteristics select signals; Clamp, Data.

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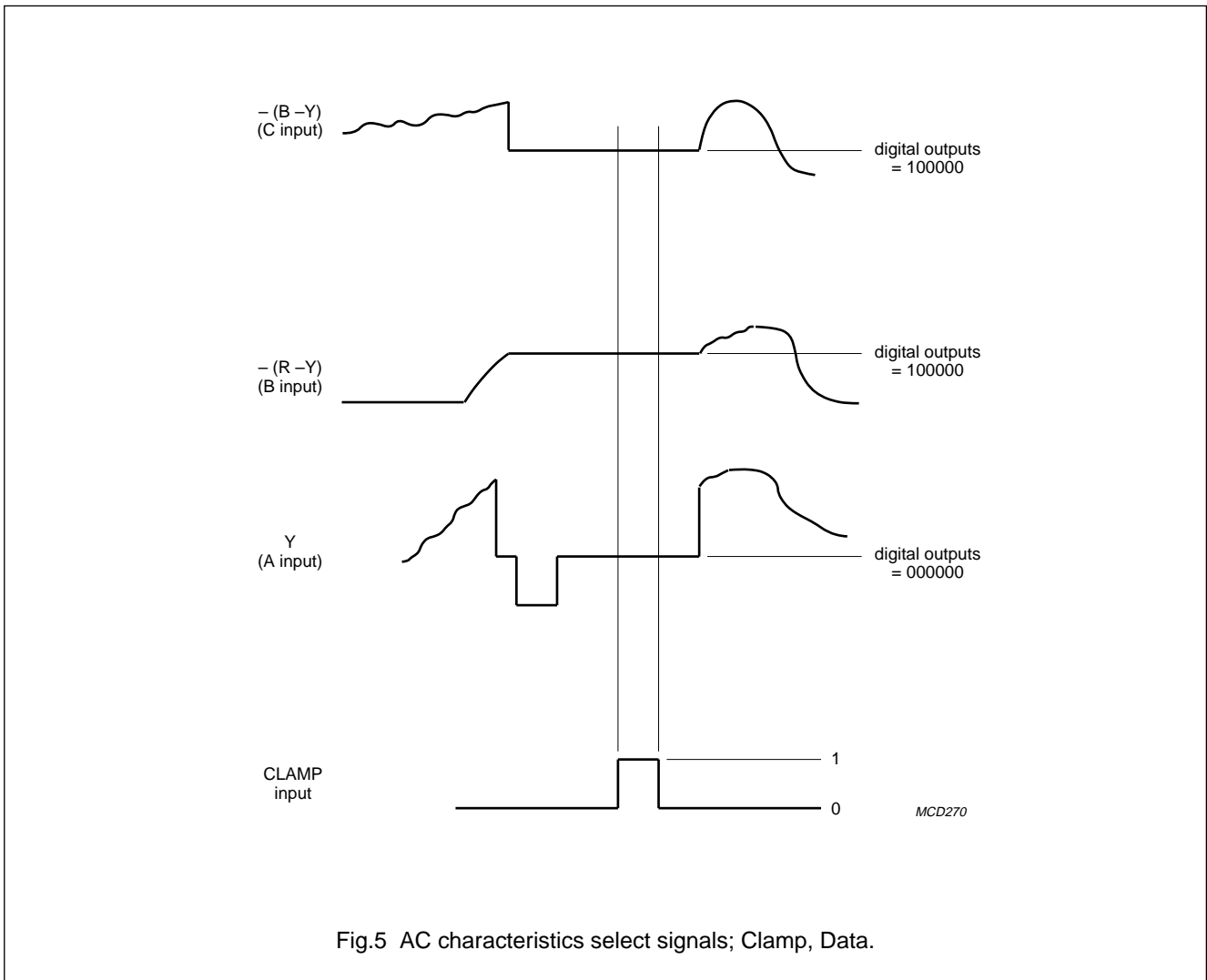


Fig.5 AC characteristics select signals; Clamp, Data.

**Table 5** Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
Clamping time per line (signal active)	2.2	3.0	3.3	$\mu$ s
Input signals clamped to correct level after	-	3	10	lines

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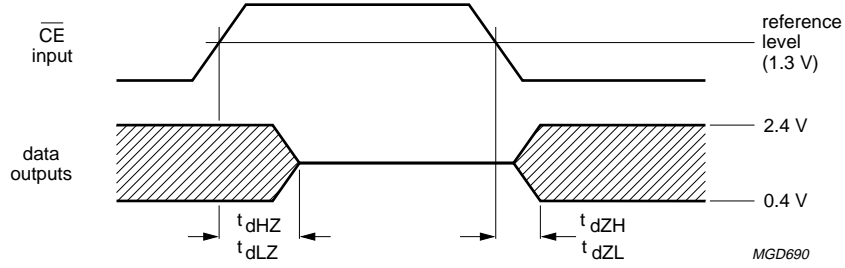


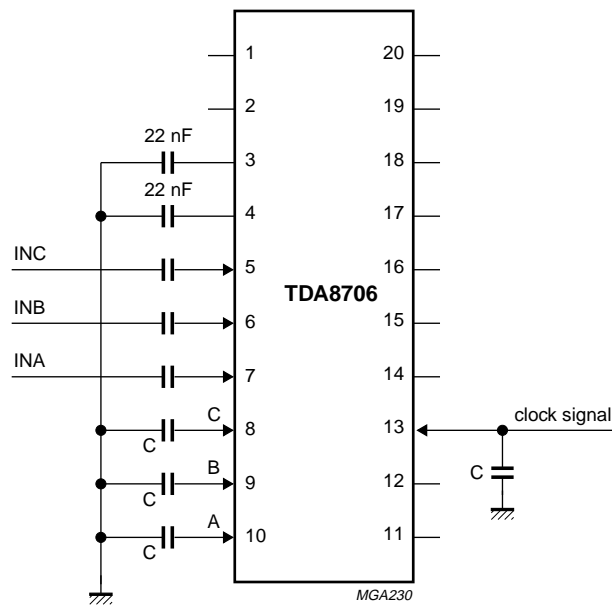
Fig.6 Timing diagram of 3-state delay.

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## APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote reference number FTV/9112).



- (1) 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins.
- (2)  $V_{RB}$  and  $V_{RT}$  are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity.
- (3) Analog and digital supplies should be separated and decoupled.

Fig.7 Application diagram.

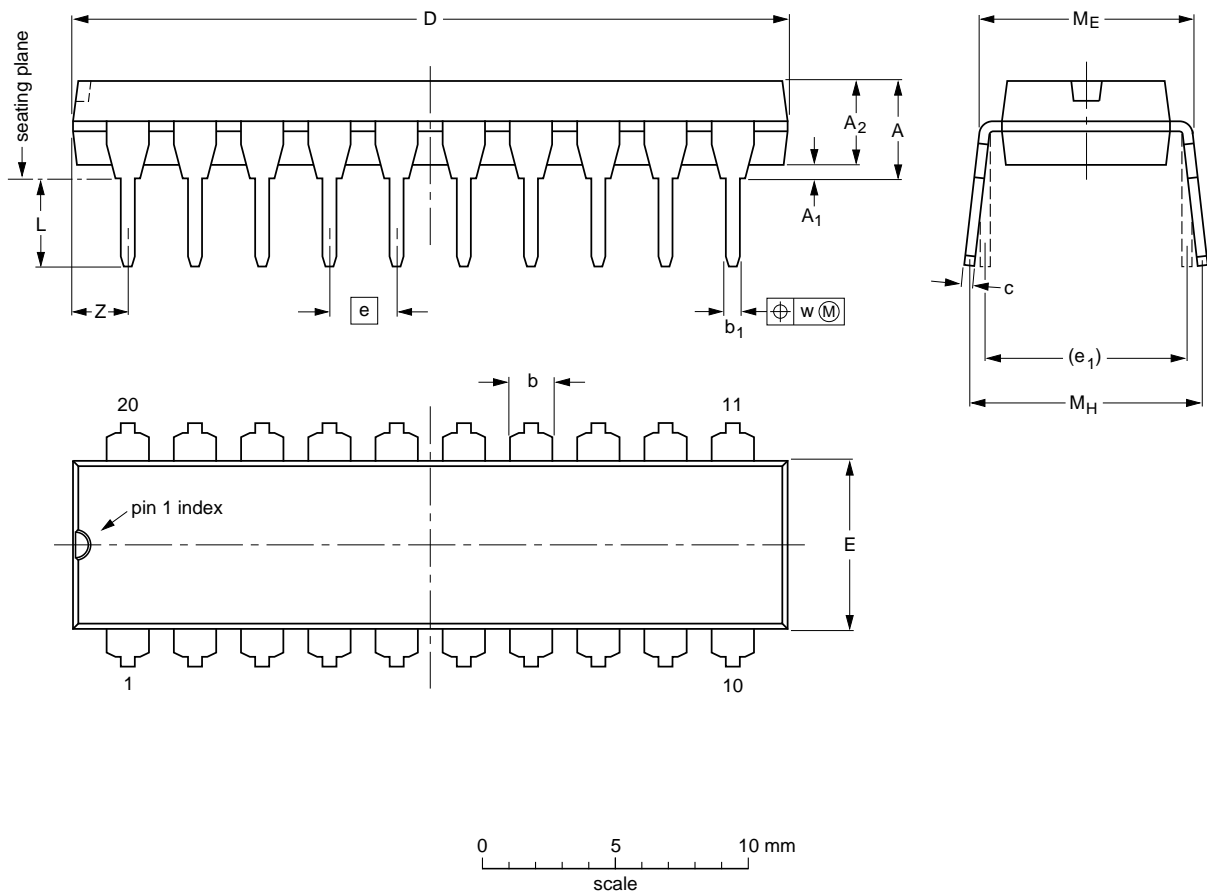
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## PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

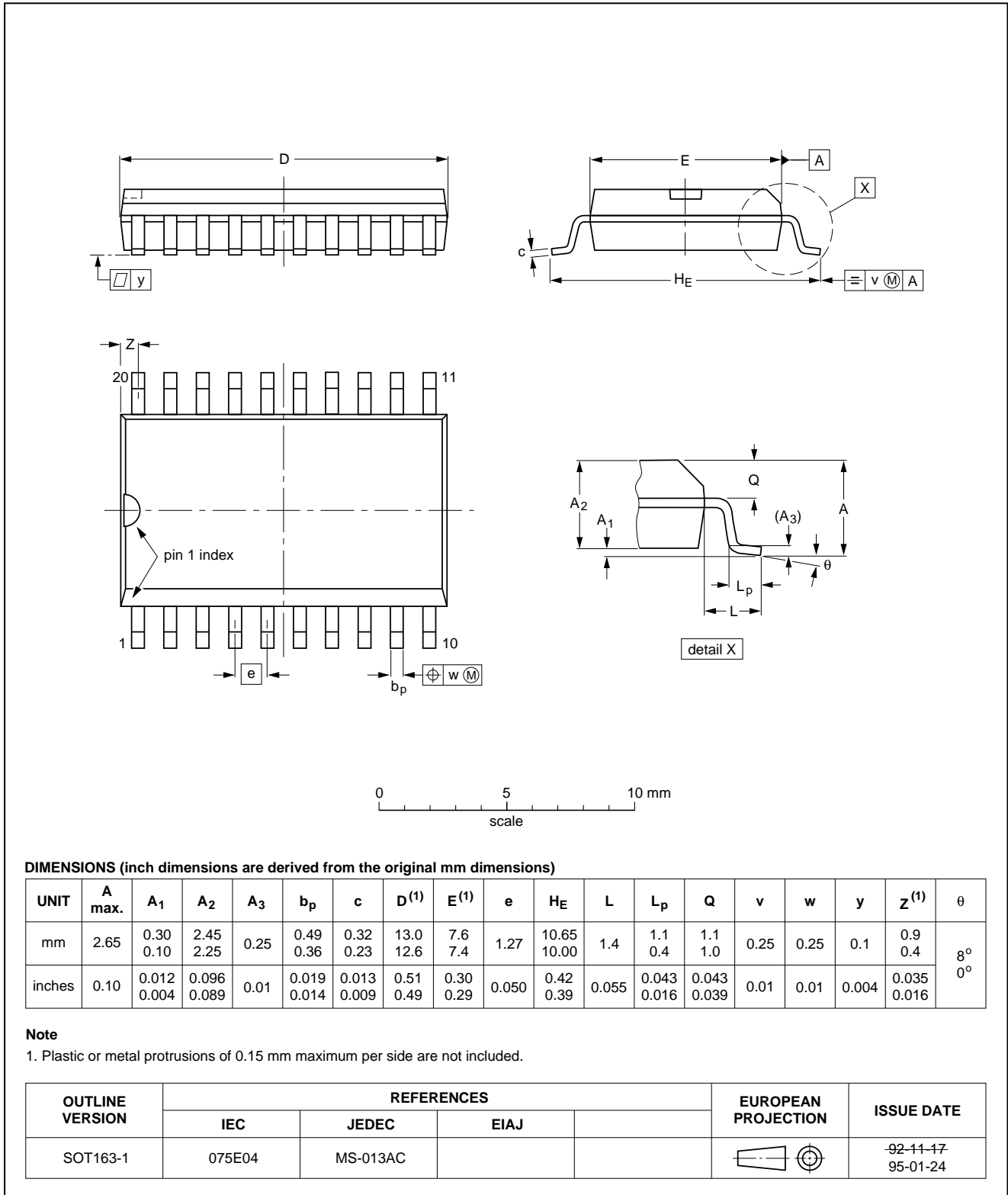
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



## 6-bit analog-to-digital converter with multiplexer and clamp

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.